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Amendment and listing of the claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A multi-chassis broadcast router, comprising:

a first chassis in which a first routing engine and at least one clock-demanding component reside;

a second chassis in which a second routing engine and at least one clock-demanding component reside;

a first link coupling an input side of said first routing engine residing in said first chassis and an input side of said second routing engine residing in said second chassis; and

a master clock residing in said first chassis, said master clock coupled to said at least one clock-demanding component residing in said first chassis and to said at least one clock-demanding component residing in said second chassis via said first link, said master clock supplying said at least one clock-demanding component residing in said first chassis and said at least one clock-demanding component residing in said second chassis with a common clock signal.

2. (Currently Amended) The ~~apparatus~~ router of claim 1, and further comprising:

a first router matrix card supportably mounted by said first chassis, said first routing engine and said master clock residing on said first router matrix card; and

wherein said at least one clock demanding component residing in said first chassis further comprises at least one input card.

3. (Currently Amended) The ~~apparatus~~ router of claim 1, and further comprising:

a third chassis in which a third routing engine and at least one clock--demanding component reside;

a second link coupling said input side of said first routing engine residing in said first chassis and an input side of said third routing engine residing in said third chassis, said master clock residing in said first chassis coupled to said at least one clock-demanding component residing in said third chassis via said second link;

wherein said master clock residing in said first chassis supplies said at least one clock-demanding component residing in said third chassis with said common clock signal ~~through~~.

4. (Currently Amended) The ~~apparatus~~ router of claim 3, and further comprising:

a third link coupling said input side of said second routing engine residing in said second chassis and said input side of said third routing engine residing in said third chassis;

wherein said first routing engine residing in said first chassis, said second routing engine residing in said second chassis and said third routing engine residing in said third chassis are arranged in a fully connected topology.

5. (Currently Amended) The ~~apparatus~~ router of claim 4, wherein a redundant routing engine resides in each one of said first, second and third chassis.

6. (Currently Amended) The ~~apparatus~~ router of claim 5, and further comprising:

a fourth link coupling an input side of said redundant routing engine residing in said first chassis to an input side of said redundant routing engine residing in said second chassis;

a fifth link coupling said input side of said redundant routing engine residing in said first chassis to an input side of said redundant routing engine residing in said third chassis; and

a sixth link coupling said input side of said redundant routing engine residing in said second chassis to said input side of said redundant routing engine residing in said third chassis;

wherein said redundant routing engine residing in said first chassis, said redundant routing engine residing in said second chassis and said redundant routing engine residing in said third chassis are arranged in a second fully connected topology.

7. (Currently Amended) A multi-chassis broadcast router, comprising:

a first chassis, said first chassis supportably mounting a first router matrix card, a redundant router matrix card, at least one clock-demanding input card and at least one clock-demanding output card;

a second chassis, said ~~first~~ second chassis supportably mounting a first router matrix card, a redundant router matrix card, at least one clock-demanding input card and at least one clock-demanding output card;

a first master clock residing on said first router matrix card supportably mounted within said first chassis, said first master clock coupled to said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said first chassis and to said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said second chassis, said first master clock supplying said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said first chassis and said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said second chassis with a common clock signal;

a second master clock residing on said redundant router matrix card supportably mounted within said second chassis, said second master clock coupled to said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said first chassis and to said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said second chassis, said second master clock supplying said at least one clock-demanding input card

and said at least one clock-demanding output card supportably mounted by said first chassis and said at least one clock-demanding input card and said at least one clock-demanding output card supportably mounted by said second chassis with a redundant common clock signal; and

control logic coupled to said first master clock and said second master clock, said control logic determining whether said first master clock should issue said common clock signal or whether said second master clock should issue said redundant common clock signal.

8. (Currently Amended) The ~~apparatus~~ router of claim 7, wherein said control logic has a first input coupled to said first router matrix card supportably mounted by said first chassis and a second input coupled to said redundant router matrix supportably mounted by said second chassis, said control logic determining, based upon a first signal received via said first input and a second signal received via said second input whether said first master clock should issue said common clock signal or whether said second master clock should issue said redundant common clock signal.

9. (Currently Amended) The ~~apparatus~~ router of claim 8, wherein:

a first routing engine and a first transmission expansion port reside on said first router matrix card supportably mounted by said first chassis; and wherein:

a second routing engine and a second transmission expansion port reside on said redundant router matrix card supportably mounted by said second chassis.

10. (Currently Amended) The ~~apparatus~~ router of claim 9, wherein:

said first input to said control logic is coupled to said first routing engine residing on said first router matrix card supportably mounted by said first chassis and said second input to said control logic is coupled to said second routing engine residing on said redundant router matrix card supportably mounted by said second chassis; and wherein

said control logic has a third input coupled to said first transmission expansion port residing on said first router matrix card supportably mounted by said first chassis and a fourth input coupled to said second transmission expansion port residing on said redundant router matrix card supportably mounted by said second chassis

said control logic determining, based upon said first signal received via said first input, said second signal received via said second input, a third signal received via said third input and a fourth signal received via said fourth input, whether said first master clock should issue said common clock signal or said second master clock should issue said redundant common clock signal.

11. (Currently Amended) The ~~apparatus~~ router of claim 10, wherein said control logic further comprises:

a first state machine residing on said first router matrix card supportably mounted by said first chassis;

a second state machine residing on said redundant router matrix card supportably mounted by said second chassis;

said first state machine determining, based upon said first signal received via said first input, said second signal received via said second input, said third signal received via said third input and said fourth signal received via said fourth input, whether said first master clock should issue said common clock signal; and

said second state machine determining, based upon said first signal received via said first input, said second signal received via said second input, said third signal received via said third input and said fourth signal received via said fourth input, whether said second master clock should issue said redundant common clock signal;

wherein only one of said common clock signal and said redundant common clock signal can be issued at one time.

12. (New) A method comprising:

supplying a common clock signal from a master clock, said master clock residing in either a first chassis or a second chassis of a multi-chassis broadcast router, the common clock signal being supplied via a link to (1) at least one clock-demanding component residing in said first chassis and (2) at least one clock-demanding component residing in said second chassis, the link coupling an input side of a first routing engine residing in said first chassis and an input side of a second routing engine residing in said second chassis.

13. (New) The method of claim 12, wherein:

said first chassis comprises a router matrix card, and the router matrix card includes a master clock and the first routing engine,

said second chassis comprises a router matrix card, and the router matrix card includes a master clock and the second routing engine, and

the method further comprises determining whether to supply said common clock signal from said master clock in said first chassis or from said master clock in said second chassis.